

# Solving SoC Design Challenges with ARM® Hard Macrocells

By Sumit Sahai, Product Manager, Processor Division, ARM

The ARM® Hard Macro portfolio offers performance and power optimized hard macrocell implementations of the Cortex™-A series processors.

For SoC designers willing to make a trade-off between the multifaceted flexibility offered by the traditional RTL-based SoC development strategy and the significant costs and efforts it involves, the ARM Hard Macro portfolio is an exciting alternative strategy which enables higher profitability through benchmarked PPA (Performance, Power, and Area), design risk reduction and faster time-to-market.

## SoC Development Strategies

In the early days of processor licensing at ARM, the primary deployment model was the hard macro. Synthesis, place and route were yet to become the commonly used techniques that they are today. As a result, most of the design work was done in schematics and custom layout.

Since then, the industry has moved to a more rapid and flexible design flow based around RTL design and EDA tools for synthesis, place and route. ARM has kept pace with the industry, and in the last decade the majority of the ARM customers have licensed soft-core deliverables. Using a combination of the ARM reference flow deliverables and their own internal flows, silicon vendors have typically built their own implementations from the ARM RTL deliverables.

Today, SoC designers working on ARM processors have several design strategies to choose from:

- Soft-core, or RTL implementation
- Supplementing RTL implementation with ARM Processor Optimized Packs (POP)



- Supplementing RTL + POP implementation with ARM ActiveAssist design consultancy
- Using ARM Hard Macrocells

## Soft-core implementation

SoC designers typically take the ARM RTL, along with scripts, constraints and the floor plan through several iterations of the complete implementation flow until the macrocell achieves the desired PPA. In addition to the ARM IP, high performance libraries from a foundry may sometimes be utilized at an additional cost to boost PPA characteristics.

ARM soft-core products offer silicon licensees the ultimate flexibility in terms of:

- **RTL configuration:** Most of the ARM CPU products offer configuration options including L1 or L2 cache size, number of interrupts to be supported, L1 parity support, L2 ECC support, the number of CPUs in an MP cluster, etc.
- **Floor plan:** Licensees get to design their floor plan to suit their SoC floor plan. While ARM provides certain floor planning recommendations, silicon licensees have the option to explore their own floor plan based on their specific configuration and the IP they plan to use.
- **IP selection:** Most licensees have access to a range of Physical IP from various sources such as ARM, their own internal IP or IP from other providers.
- **Vt or channel lengths selection:** Licensees have complete freedom to choose the appropriate mix of Vt cells and the preferred channel lengths to achieve the target PPA.
- **PPA targets:** Licensees get to make significant trade-offs in area, power and performance depending on the target markets and applications. For example, the same RTL can be used to build a 2GHz frequency design on a high speed process with an obvious leakage penalty or a 1GHz design on a low-leakage process.
- **Process choice:** Licensees can take their designs to foundries of their choice.

This multifaceted flexibility allows ARM licensees to deploy differentiated CPU offerings across a range of target markets and applications.

While the above methodology offers the designers complete freedom over the design parameters, it also requires significant investment in terms of cost, expertise and effort.

### Supplementing soft-core implementation

ARM high-performance PIPD libraries provide a useful option for silicon vendors looking to enhance the device's PPA characteristics. Use of the ARM PIPD libraries and POPs (Process Optimized Packs) enhances performance capability and reduces design time. SoC designers still need to invest effort in order to get optimal results.

Additionally, SoC designers may choose to use ARM Active Assist. Active Assist provides a design evaluation and consultancy service for licensees looking to fine tune enhanced target characteristics e.g. high performance, reduced area or power, etc.

### Using ARM Hard Macrocells

While soft-core implementation remains the best choice for design teams wanting complete freedom and flexibility, some recent industry trends are making designers look at alternatives.

- **Increasing SoC Complexity** – The complexity of a typical SoC has increased multi-fold over the last few years. Instead of a uni-core design, many SoC now feature dual or quad cores. The target maximum frequency has shot up steadily, while

geometries are getting smaller. A few years ago, designers who were working on a uni-core SoC on 40 nm targeting a maximum frequency of 600 MHz are now perhaps looking at the prospect of implementing a quad core on 28-20 nm targeting in excess of 2 GHz.

- **Tightening markets** – Markets are getting extremely competitive, with several solutions and players trying to carve out a healthy share. The battle for the highest rated maximum frequency is sometimes fuelled more by marketing hype than by the target applications, but remain a real requirement.
- **Time-to-Market pressures** – Design teams are now working under extreme time-to-market pressures due to the high rewards for getting to market early. Conversely, the consequences of delays in product launch can be crippling.
- **Risk and cost barriers of entry** - Design teams are inhibited by the high costs and risks associated with adopting new technology, or entering new markets.

In order to maximize their ROI in very competitive markets, SoC designers are focusing on:

- Device differentiation
- Achieving the optimal PPA
- Reducing costs and risks
- Getting to the market in time

Failing in any one of these could potentially lead to serious business fallout, both for market leaders and those seeking new markets.

ARM Hard Macros provide a way for SoC designers to combat these market pressures through guaranteed PPA, reducing the cost, effort and risk associated with the design and by enabling faster time-to-market.

## Solving the SoC Design Challenges

Let us consider some of the technical challenges faced by today's SoC designers, and how ARM Hard Macros help overcoming these.

- **ARM architecture knowledge:** As the ARM architecture becomes increasingly pervasive throughout the spectrum of digital devices, the number of design teams working globally on the ARM architecture is growing proportionally. Some design teams are within companies that have no prior ARM experience while others are divisions within organizations that have prior ARM experience in other markets but are now broadening their use of ARM products to new applications.
  - ARM Hard Macros provide an easy, low cost, low risk entry into the ARM architecture for design teams new to ARM.
- **Processor knowledge:** During the development of the RTL IP, ARM builds up a substantial amount of expertise through

implementation trials. While ARM RM (Reference Methodology) allows licensees to come up to speed on the processor, the inherent expertise developed within ARM cannot be captured so succinctly, thereby leaving a big learning curve for a licensee to climb.

- ARM Hard Macros utilize processor IP, POP and the 'secret sauce' (the internal ARM expertise) to the fullest extent possible, allowing for highly optimized designs that often exceed the results licensees obtain after significant efforts.

- **Tools and implementation expertise:** Designing best-in-class devices requires significant expertise in implementation technology and tools. Newer teams take time to build up this expertise in house. Even major silicon vendors tend to have the expertise concentrated within one or two technical leadership groups or geographical design centers, with the other divisions within the organization either having to reuse implementations which may not be an exact fit for purposes or having to borrow expertise to do their own specific implementations.

- ARM Hard Macros enable licensees to overcome any shortcomings in implementation and tools expertise without compromising on features, PPA and/or quality, and allow them to focus on adding value and differentiation.

- **Mastering new geometries:** When moving to new geometries and libraries, designers have to get acquainted with the intricacies of the new nodes. The nature of cell libraries and their leakage characteristics vary widely between 40, 32 or 28 nm nodes.

- ARM Hard Macros provide guaranteed PPA, and significant risk reduction and faster time-to-market for licensees designing on newer geometries.

- **Selecting the optimal PPA balance:** SoC implementation often involves a delicate and difficult balancing act between the conflicting demands of maximizing frequencies and maintaining low power levels. Often, PPA targets are determined by technical requirements such as HD video decoding or encoding, browsing web pages, etc. Frequency targets are often also being driven by marketing needs, as vendors compete to introduce devices with the highest GHz rating into the market. Getting the PPA balance wrong can seriously affect market success.

- ARM Hard Macros provide licensees with finely balanced solutions which take away the risks, uncertainties and guesswork involved in achieving high frequency with low power.

- **Achieving the optimal PPA balance:** Nailing down the desired PPA to succeed in the market is only the first step. It subsequently takes significant effort to actually hit these targets, involving several iterations of fine tuning and benchmarking, but there is no real guarantee of success until engineering is complete.

- ARM Hard Macros leverage leading edge Physical IP Processor Optimization Packages to deliver outstanding PPA characteristics, even before the device is developed, providing a highly competitive market advantage. This advantage is

further amplified by the simplification of the design cycle and faster time-to-market.

- **Assembling the complete solution:** Designers need to integrate several IP such as RTL and POP, and work with multiple tools to achieve the best results. They also have to implement complex optimization techniques and fill in the gaps in the RTL IP themselves, such as insert power domains, DFM/DFT, using mixed Vt libraries and finding ways to reduce leakage and dynamic power.

- ARM Hard Macros provide the complete solution – pre-integrated processor IP, POP, power domains, clock tree insertion, DFM/DFT and more into one package that can be dropped into the SoC design easily and quickly.

For designers new to ARM, ARM Hard Macros provide an attractive low risk, low cost and proven entry point into the ARM architecture. For existing licensees of Classic ARM processors (ARM7™, ARM9™ and ARM11™), ARM Hard Macros provide an accelerated upward migration route by reducing the cost, effort and risk.

For existing licensees of ARM Cortex-A processors, ARM Hard Macros enable quick market penetration with a first generation device, in parallel to the development of the second generation device using a soft-core. Hard Macros also provide a lifeline for secondary divisions lacking in sufficient expertise to do their own soft-core implementations and having to do with devices made for and by the primary divisions.

So, we can conclude that irrespective of the designers' level of experience with the ARM architecture, the ARM Hard Macro products provide a useful option for those looking beyond the traditional SoC development model.

### ARM Expertise through the Design Phase

Designers encounter several decision points during SoC design. Seen individually, some of these decision points and their effect on the final PPA may seem minor or even unquantifiable. But making the right choices at every stage could potentially provide a significant cumulative improvement to the PPA. Often, the difference between a highly optimized design and a moderately optimized one can be attributed to a handful of design decisions. Without the detailed processor knowledge and tools expertise that ARM has, designers may have to resort to costly trial and error.

Experienced designers are also well versed with the 80-20 rule. The 80-20 rule is applicable to several models and situations, but specifically in terms of implementation challenges we can paraphrase this to – 'It can take as much as 80% of the design effort to squeeze out the last 20% of performance.'

Let us have a closer look at how ARM expertise can provide an edge at every stage of the design and implementation phase, leading to a highly optimized hard macrocell that typical SoC design teams may struggle to achieve within similar time frames and costs.

<b>RTL Configuration</b>		
<b>RTL Configuration Task</b>	<b>Challenges</b>	<b>ARM Hard Macro Benefit</b>
Configure RTL with desired options	Designers need to determine the right options.	ARM Hard macros are standard 'signature' implementations, built with the most likely options thereby reducing risk and maximizing the application envelope.
	Designers need time and assistance to decode the multitude of RTL switches to avoid errors.	ARM has sound knowledge of all the switches, and ARM Hard Macros reduce risk of errors.
	Designers need to create test cases to comprehensively verify the selected configurations.	ARM Hard Macros remove the cost and time needed for verification
Instantiate memories	Designers need to select the correct memories, connect them in the net list and verify. Memory selection affects timing, area, power and routing.	ARM Hard Macros use the best suited memory configurations, taking into account the impact on PPA, etc.
	Choosing the right sizes for L1 and L2 cache.	ARM Hard Macros use the most appropriate RAM sizes based on detailed market and technical analysis.
	Designers need to do RAM integration and profiling.	ARM Hard Macros remove the cost, errors and time needed for verification.
MBIST controller	Designers need to insert MBIST controller for testing memory to ensure all the bits of memory are accessible and working correctly.	ARM Hard Macros provide MBIST support, either inbuilt or via pin outs.

<b>Synthesis</b>		
<b>Synthesis Task</b>	<b>Challenges</b>	<b>ARM Hard Macro Benefit</b>
Choose between flat or hierarchical design	Designers need to determine the best option. This needs expertise, experience and several iterations. Non-optimal designs suffer on PPA.	ARM Hard Macros use the vast ARM knowledge and experience to produce designs offering the best PPA. For example, the Gannet A5 40LP hard macro is flat, whereas the Osprey A9 40G macro is hierarchical.

DFT	Designers need to develop DFT patterns to catch manufacturing bugs in the die. Any errors in the DFT patterns may lead to post silicon debug unable to identify all defective regions.	ARM Hard Macros provide DFT.
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<b>Floor Plan &amp; Power Grid</b>		
<b>Floor Plan &amp; Power Grid Task</b>	<b>Challenges</b>	<b>ARM Hard Macro Benefit</b>
Power grid design and analysis for single power domain designs	Routing the power meshes and checking if IR targets are met. Since IR drop aware analysis is only guidance tool, designer needs to be very careful because faults are found only in silicon.	ARM knows the best ways to route the power meshes our from benchmarking and implementation trials. ARM Hard Macros remove the risk of getting it wrong.
Power grid design and analysis for multiple power domain designs	Multiple power domains and DVFS make this one of the most difficult implementation challenges, having a significant effect on PPA.	ARM Hard Macros benefit from ARM expertise in handling multiple power domains and DVFS.
	Tools have major difficulties in understanding the power intent hence designers cannot just rely on placement by tools alone because blocks may need manual placement.	ARM Hard Macros benefit from ARM expertise in manual placement to achieve the best results in terms of timing and power domains.
Develop wakeup/sleep strategy to manage inrush current	Power gating cell insertion is tricky because it is a relatively new circuit based skill.	ARM Hard Macros benefit from ARM expertise and reduce the risks.
		ARM has seen multiple cases where designers have sought ARM assistance to get this right.
Determine the number of power planes required.	Drawing the power domain boundaries, choosing the number of different voltage levels in DVFS etc are tricky design choices which have an impact on timings and verification	ARM expertise with the processor design allows us to provide the most optimized solution.

Place & Route		
Place and Route Task	Challenges	ARM Hard Macro Benefit
Balance clock skews and latency to meet PPA goals	Designers need to experiment with the clocks to reduce latency which requires expertise, experience and several iterations to find the best solution.	ARM Hard Macros benefit from significant ARM expertise to achieve the best results.

Sign-Off		
Sign-off Task	Challenges	ARM Hard Macro Benefit
Run Design rule verification checks	Several corners need to be taken care of.	ARM Hard Macros remove the cost, errors and time needed for verification.

**Summary**

The ARM Hard Macro Portfolio offers performance or power optimized hard macrocell implementations of the Cortex-A processors. These hard macros enable vendors to achieve higher levels profitability through guaranteed PPA, risk reduction and faster time-to-market, providing a winning edge in highly competitive markets.

Tapping into our vast pool of ARM processor, tools and implementation knowledge and experience, ARM Hard Macros provide finely tuned PPA results that are hard to beat using the traditional soft-core implementation strategies for all but the most experienced design teams.

**END**

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