

*Low-power design has changed the design and verification paradigm forever, and the industry is in dire need of a systematic approach to low power verification.*

# A Methodology for Low-Power Verification

By Srikanth Jadcherla, Synopsys and Dave Flynn, ARM

Low-power design has changed the design and verification paradigm forever. Increased complexity and the need for accurate verification have stymied verification teams and held tapeouts at hostage. The industry is in dire need of a systematic approach to low-power verification. In response to this, ARM, Renesas Technology and Synopsys have written the Verification Methodology for Low-Power (VMM-LP), which is based on the collective experience of over 30 companies with real life low-power verification experience.

## Emergence of Low-power Designs

Until recently, the semiconductor industry was tracking the famous Moore's law, which states that the number of transistors will double with every new process technology. The implication of Moore's law is that design teams can reduce cost with successive migrations down the process technology curve. The continuation of Moore's law is therefore important for the health of the semiconductor industry.

So what finally broke the camel's back? Well, it is power. Both leakage and dynamic power are increasing with every switch to smaller process geometries. Power has broken the laws of scaling and is a large barrier to the continuation of Moore's law. Consequently, designers are battling to tame power in an effort to keep Moore's law alive.

The increasing use of handheld devices and popularity of portable appliances has placed huge demands on battery life, which in turn has driven low-power requirements. Finally, government regulations and the desire to be 'green friendly' have driven companies to reduce power.

## Impact of Low-power

Power-managed designs introduce design complexity. Low power devices typically operate under multiple voltages and frequencies to save power, and have multiple modes of operation. Designers can turn large sections of the design on or off, and dial up voltages and frequencies for performance or dial them down for power savings - either statically or dynamically. Designers may choose to retain contents of the powered down sections (domains) for quick system reboot, or place large blocks of logic or memories in a standby mode. In short, a low-power design can operate in multiple power states. Such a design transitions from one operating mode to another through one or more power states. The transitions and sequences of transitions are very important for correct functional behavior of the design. Unwanted transitions and sequences can easily result in a malfunctioning or non-functioning low-power design.

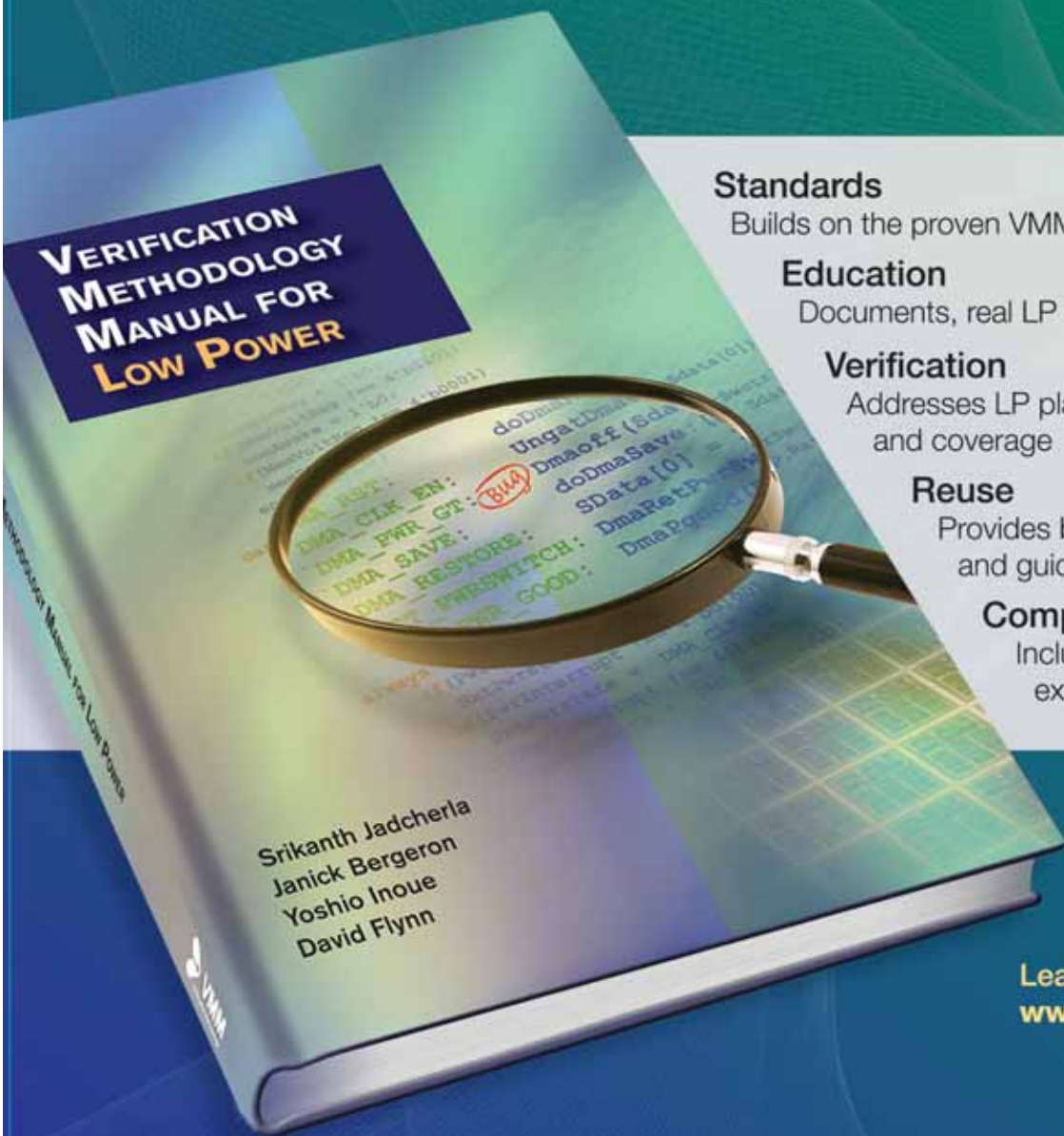
Regardless of what designers do to conserve power, it almost always introduces new bugs. They can inadvertently introduce bugs in the low-power design elements that are added to enforce low-power functionality. Design bugs can also creep up in the control signal sequence that helps transition a low-power design from one operating mode to another. Multiple voltages transitioning at different slopes may result in incorrect operation of the device unless the voltage values are strong enough to register proper control events leading to design transitions. These bugs are not the typical design bugs in the non low-power era, but a new class of "resistant" bugs that designers must carefully avoid and definitely check before tape-out. Therefore, verification takes on a whole new meaning in the context of low-power designs.

Low-power designs have an unfortunate consequence of increasing design and verification complexity.

Introducing the VMM-LP

The industry's first

# Verification Methodology for Low Power



**VERIFICATION  
METHODODOLOGY  
MANUAL FOR  
LOW POWER**

Srikanth Jadcherla  
Janick Bergeron  
Yoshio Inoue  
David Flynn

## Standards

Builds on the proven VMM standard

## Education

Documents, real LP bug examples

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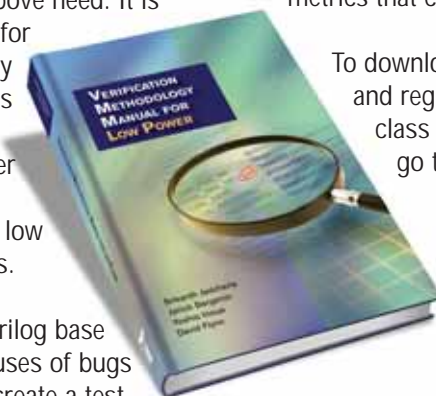


**Low-power Verification** Low-power designs have the unfortunate consequence of increasing design and verification complexity. Verification of low-power designs involves verification of the design in multiple power states, and verifying that only the intended transitions and sequences of transitions have occurred. Fortunately, low-power verification tools have risen to the challenge and there are now voltage-level aware simulation products such as MVSIM with VCS® from Synopsys that can accurately verify the functionality of these designs. Static checkers such as MVRC from Synopsys verify that implementation tools follow the power specification and report any mismatches if present.

**Need for a Verification Methodology for Low Power** However, tools alone are not sufficient. First, the low-power designer needs to understand the impact of low-power designs, the common causes of bugs, and the ways to avoid them. Second, the verification team supporting a low-power design needs to understand how to plan and execute a verification effort centered on low-power. They need to come up with a low-power specific test plan that effectively exercises the low-power modes of a design and puts it to the litmus test. Third, the verification team needs a way to calibrate their test plan, to gauge its effectiveness, to understand the progress of their verification efforts, and to come to a verification closure for their design. Finally, the verification infrastructure used in one design needs to be repeatable across multiple low-power designs. The last requirement implies the need for a reusable architecture that companies can easily deploy across design teams to leverage the best practices learned from one verification project to another. The end result is a need for a robust, structured, repeatable verification methodology for low-power.

**Introducing Verification Methodology Manual for Low-power (VMM-LP)** The Verification Methodology Manual for Low-power addresses exactly the above need. It is built on the popular and widely deployed VMM for SystemVerilog developed and released earlier by ARM and Synopsys. Authored by ARM, Renesas Technology, and Synopsys, and including contributions from verification experts from over 30 companies, it is an industry first initiative to define and document a blueprint for successful low power verification based on real life experiences.

The VMM-LP consists of a book and SystemVerilog base classes. The book documents the common causes of bugs in low-power designs, a step-by-step guide to create a test infrastructure for low power verification, rules and guidelines for verification, recommendations based on industry best practices, and a section on how to evaluate a testplan.



The base classes provided as part of the VMM-LP help to create a repeatable, scalable, verification infrastructure that companies can deploy within different teams within the same organization. The book is available now as a hardcopy through Amazon.com or as a PDF download from the Synopsys website for customers of Synopsys.

### The Authors

The lead authors of the VMM-LP are Srikanth Jadcherla, Group Director of Research and Development at Synopsys. Srikanth was the founder of ArchPro Design Automation, which Synopsys acquired in 2007; Janick Bergeron, Synopsys Fellow and moderator of the Verification Guild website; Yoshio Inoue, Chief Engineer, Design Technology Division, Renesas Technology Corp., and David Flynn, ARM Fellow and coauthor of the "Low Power Methodology Manual" (LPMM) published by Springer.

### Summary

The VMM-LP has drawn on industry-wide expertise to define a robust and scalable verification architecture that design teams and verification engineers can use to complete the verification of advanced low power designs. The methodology addresses all aspects of functional verification of power management functions, including suggestions for static versus dynamic verification, design-for-verification techniques, and best-practice use of assertions and coverage metrics that can help to achieve rapid verification closure.

To download free PDF of the VMM-LP book and register to be notified when VMM-LP base class library source code becomes available, go to [www.vmmcentral.org/vmmlp](http://www.vmmcentral.org/vmmlp).

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*VMM-LP offers best practices for low-power verification*

**END**