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## Cost Efficient ARM processor-based Custom SoCs for Fabless Semiconductor Companies

By Jay Johnson, Atmel

Fabless semiconductor companies are often stuck between a rock and a hard place when it comes to implementing new designs. FPGAs with embedded soft core or external microcontroller are not an option for fabless IC companies because the company's "secret sauce" is vulnerable to theft and cloning when implemented in an FPGA. In addition FPGAs have poor performance and power characteristics. FPGAs typically consume 44-times more power and operate at about 1/8 the speed of an integrated SoC.

Although a full-custom ASIC would be the preferred solution, the high non-recurring engineering (NRE) costs and minimum order quantities of 100,000-plus units are prohibitive - particularly when market acceptance is uncertain. NREs for a bare bones 0.13 micron design run about \$350,000. For a state-of-the-art 45 nm design NREs are over \$1M.

Another factor to consider is the life cycle of the end product versus the one-year development time of a full-custom ASIC. Product life cycles are often as short as six months. It takes longer to develop a full-custom ASIC than the life of many end products. This situation makes it impossible to achieve the cost, power and performance benefits of custom ASICs.

Another option is low-volume, quick-turnaround ASICs that can be fabricated in four to six weeks. These ASICs utilize a direct-write electron beam to customize a single via layer, thereby eliminating the need for any custom mask charges.

Although there are no NRE charges with this type of ASIC, "hidden" fees to license the processor IP can be hundreds of thousands of dollars, often offsetting the zero-NRE. At \$100 or more, unit costs represent another barrier to this type of solution. They are five to ten times too expensive to afford any market penetration to a fabless IC company.

A fourth option is a customizable microcontroller, based on Atmel's second generation metal programmable cell fabric (MPCF-II) technology that requires only a nominal NRE charge of just \$75k with low units costs of \$5 to \$10. Announced in 2007, the original MPCF technology achieved silicon efficiency comparable to that of cell-based ASICs (between 170K and 210K gates/mm<sup>2</sup> in 130 nm technology), which allowed low unit costs. An MPCF cell implementing a D flip-flop (DFF) versus a standard cell DFF both in a 130 nm process consumes nearly the identical area. (See Figure 1)

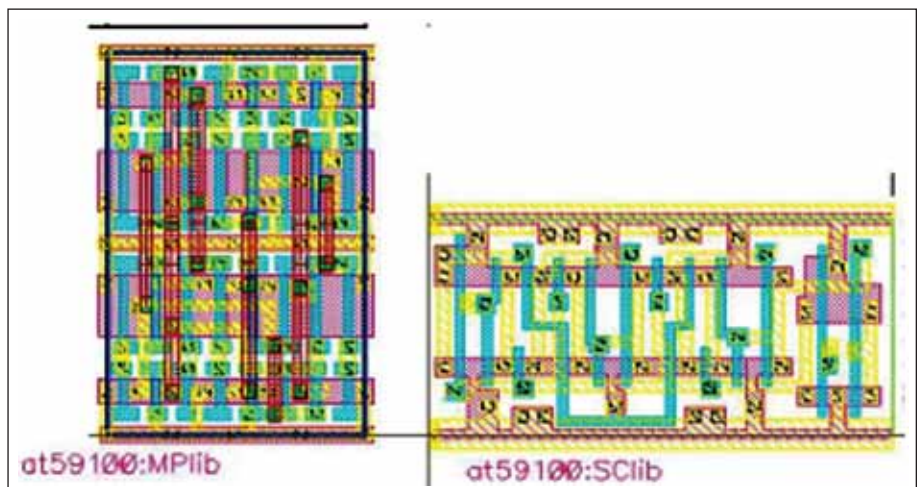


Figure 1: D-type Flip-flop in 130 nm MPCF and 130 nm Standard Cell.

NREs were minimized by implementing 85% of the die as a standard product microcontroller with an ARM7-core processor, six-layer bus, and a variety of peripherals, while leaving 15% of the die area free for customization using contact, six metal and five via layers for cell configuration and interconnect. (See Figure 2)

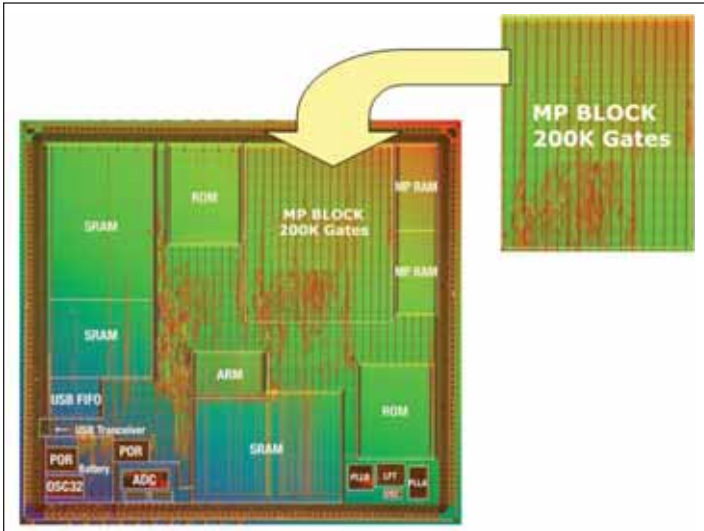


Figure 2: CAP 85%/15% Die Shot

The second generation MPCF-II technology, which is used to implement Atmel's ARM7 processor-based CAP7L customizable MCU, has a new cell library that allows the chip to be configured and routed using only three metal and three via layers, thereby reducing the number of masks from 12 to just 6 and cutting NRE costs by 50%. Thus, fabless IC companies can develop custom SoCs with no IP license fees, minimal NRE and unit costs very close to those of a full-custom ASIC.

The 85% of the die area that is predefined is a standard product microcontroller. It consists of an ARM7 core processor with 4-layer AHB bus and 22 channel peripheral DMA controller, USB device, SPI master and slave, two USARTs, three 16-bit timer counters, an 8-channel/10-bit analog to digital converter, 8-level, priority, 160 Kbytes of SRAM, a SD/MMC memory card interface (MCI) and external bus interface (EBI) that supports SDRAM, NAND flash with error code correction (ECC) and CompactFlash with True IDE mode interface to GByte-plus on-board or removable memory including USB sticks. The chip also has a fullfunctioned system controller including interrupt, power control and supervisory functions. (See Figure 3)

The 15% of the die area that is customizable contains the equivalent of 200K ASIC gates (25K FPGA LUTs), sufficient logic to implement additional processor cores, unique peripheral sets, hardware accelerators and the custom IP of the fabless semiconductor company. For example, Silicon Valley-based Amulet Technologies, a fabless vendor of interactive GUI ICs, has used the MP block on Atmel's CAP7 customizable microcontroller to integrate its proprietary Graphical Operating System, GUI engine, LCD Controller and touch interface, with the ARM7 core. Using this platform, Amulet easily can customize individual GUI ICs for high-volume manufacturers of white goods and other end-products. (See Figure 4)

In addition to providing the license-free ARM processor core, Atmel has a large library of license and royalty-free IP that has been fully verified and tested in the CAP7L MP block, and in Atmel's standard microcontrollers. Atmel's free IP includes USART's supporting RS232, RS485, ISO7816, IRDA, serial synchronous controller, I<sup>2</sup>S, Audio AC'97 controller, two wire interface (Master & Slave), serial peripheral interface (SPI), SD Card / MMC Card host controller, controller area network 2.0B + 8 mailbox (CAN), parallel I/O (32), timer counter, pulse width modulation (PWM), data encryption standard (TDES-133 MHz), advanced encryption std (AES-128/196/256), secure hash algorithm (SHA1), AHB/APB bridge, external bus interface, external static RAM/flash controller, error correction controller (ECC) for NAND Flash, SDRAM controller, and ZBT RAM controller.



Figure 4: Amulet GUI\_IC

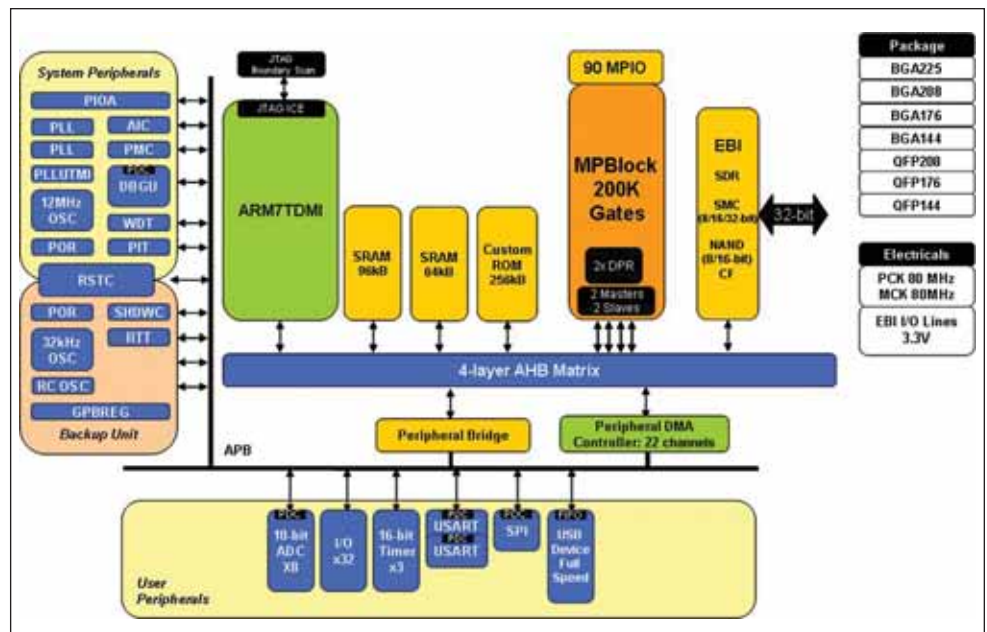


Figure 3: CAP7L Block Diagram

To ensure adequate communication between the custom functionality in the MP block and the rest of the chip, the metal programmable (MP) block has two AHB masters and two AHB slaves, fourteen advanced peripheral bus (APB) slaves, and 32-bit programmable I/O that may be hardware selected to share I/O. An on-chip priority interrupt controller provides up to 13 encoded interrupts and two additional un-encoded interrupts for DMA transfers. Multiple distributed single- and dual-port RAM blocks can be tightly coupled to the logic elements. The MP Block is supplied by all the clocks originating from the clock generator and power management controller on the customizable MCU.

Simple DMA is implemented in every peripheral on the chip, and managed by a peripheral DMA controller that off loads data moving tasks. The EBI is extremely useful in applications, such as Amulet's GUI ICs, that require huge amounts of frame buffer memory to refresh the 24-bit color VGA (640x480 pixels) LCD display. The 1.2 MByte frame-buffer is stored in external RAM and fetched from the EBI. The data transfer task is off-loaded from the ARM7 CPU to two DMA masters added to the MP block on the customizable MCU which can achieve the required data rate of 73 Megabytes per second (1.2 MBytes of data 60 times per second). ( See Figure 5)

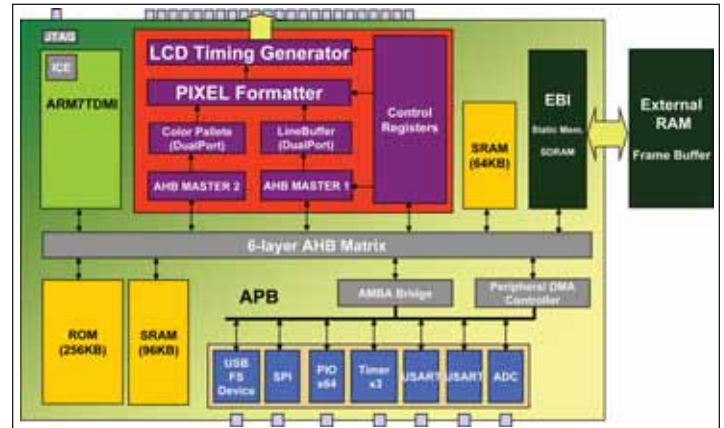


Figure 5: Amulet Block Diagram

**Design Flow** The design flow for the CAP7L is the same as it would be for an FPGA-plus-MCU or ASIC implementation. The design is initially developed using an Altera or Xilinx FPGA and an ARM7 MCU. Atmel provides the CAP7E ARM7 processor-based MCU with direct FPGA interface for this purpose. The interface on the CAP7E affords the FPGA direct access to the AHB and peripheral DMA controller on the CAP7L. Atmel also provides FPGA logic that decodes and encodes the bus traffic that flows between the FPGA and the CAP7E microcontroller.

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The logic blocks inside the FPGA are connected to the CAP7E via the AHB master and slave channels and APB slave channels. The CAP7 family remains the only ARM7 processor-based microcontroller on the market with AHB bus implementations, which can dramatically improve performance in the system. In addition, a CAP7E-plus-FPGA implementation can be used for early market testing and proof-of-concept, prior to migrating to the CAP7L.

The HDL code for any custom-IP is developed using standard, vendor-specific or third-party FPGA design tools. Once verified, the customer need only provide the register transfer level (RTL) netlist to Atmel for implementation in the MP block on the CAP7L. (See Figure 6)

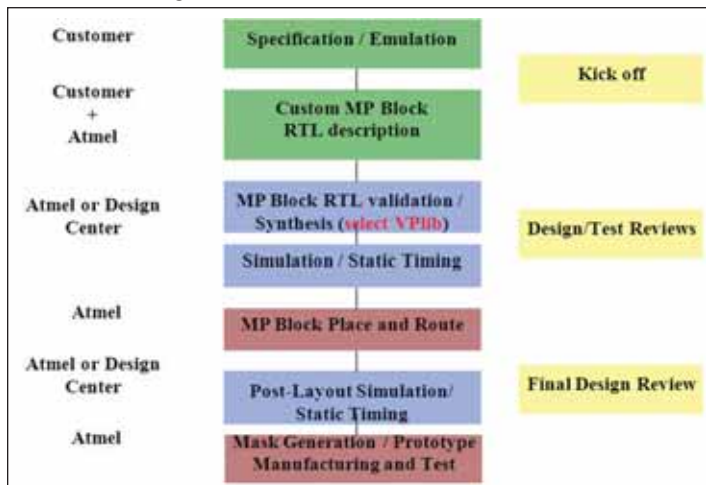


Figure 6: Design Flow

Atmel offers the AT91CAP7X-DK development kit that can be used for the co-design of the hardware and software. The kit includes a motherboard with power supply connector, TFT Color LCD display, and interfaces to the peripheral set on the AT91CAP7 customizable MCU. Motherboard features include both a USB full-speed host and USB 2.0 high-speed device, 10/100 Ethernet MAC, image sensor interface, I<sup>2</sup>S audio codec, 2.0A and 2.0B CAN controller, TFT LCD controller, MCI, SSC, PWM, LCD and AC97 controllers, SPI master and slave, two USARTs, three 16-bit timer counters, and an 8-channel, 10-bit analog to digital converter. An SD/MMC memory card interface (MCI) and external bus interface (EBI) support SDRAM, NAND Flash with error code correction (ECC) and CompactFlash with True IDE mode interface to GByte-plus on-board or removable memory including USB sticks. (See Figure 7). The motherboard also has a DBGU serial communication port, four analog inputs, a second full-speed Host USB interface, two additional USB device PHY interfaces with USB B connectors, two 3.5 mm audio jack connectors, three 3.5 mm audio jack connectors with three status LEDs, two SD/MMC card slots, TWI serial EEPROM, image sensor expansion connector, 16 button keypad, software controlled Power LED, two general-purpose LEDs, four PIO expansion connectors, and extension connectors for PCI64 FPGA I/O and mezzanine boards.

A CAP7-specific mezzanine board includes the AT91CAP7S MCU and FPGA with 80K logic elements. This plugs directly onto the motherboard for not only software and hardware development, but also connection to real world applications for prototyping and end product evaluation.

A memory expansion board includes 64Mbytes of SDRAM, 8Mbytes of NOR Flash and 256Mbytes of NAND Flash. Existing FPGA designs can be ported directly to the development board and new designs can be created using it.



Figure 7: Development Board

Atmel uses the customer's RTL to synthesize the gate-level netlist for the MP block in the customizable MCU and verifies timing. There is no customer-side ASIC engineering involved at all. The customer only needs to simulate their own IP in the CAP netlist, to verify functionality. Atmel does the rest. Prototypes are available in less than twelve weeks after the final CAP gate-level netlist is completed.

Prototypes are available within 10 weeks of final gate level netlist and production quantities within 12 weeks. The same C-compilers, RTOS, OSs, ICEs and IDEs used with Atmel's ARM-based MCUs can be used with the CAP versions of the devices. These include Atmel's free GNU gcc C compiler, GNU gdb debugger, FreeRTOS.org real-time kernel. Commercially available tools include Green Hills (Multi IDE, TimeMachine™, Integrity OS), IAR (C compiler - Embedded Workbench™), ExpressLogic (Real-time Operating System - ThreadX®) and Micrium (Real-time Operating System - μCOS/II).

**Conclusion** Second generation metal-programmable cell fabric (MPCF-II) technology offers fabless IC vendors a cost effective means of developing custom ARM processor-based SoC, with nominal NRE charges, unit costs and performance comparable to fullcustom ASICs, and no license fees.

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